FIG. 1

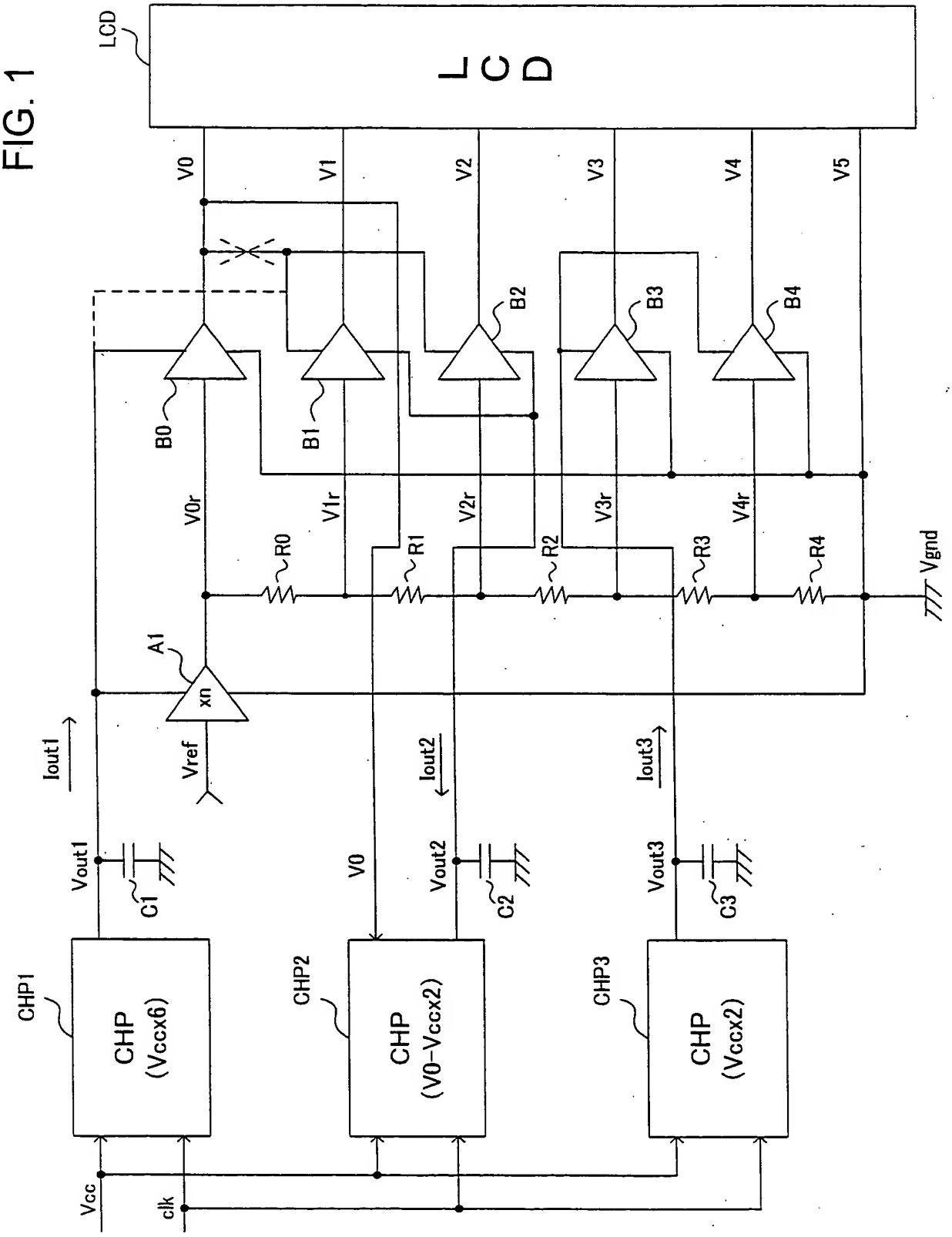
LCD
LCD
V0
V1
V2
V3
V4
V5
B0
B1
B2
B3
B4
V0r
V1r
V2r
V3r
V4r
R0
R1
R2
R3
R4
Vgnd
A1
xn
Vref
Iout1
Iout2
Iout3
Vout1
Vout2
Vout3
C1
C2
C3
V0
CHP1
CHP
(Vccx6)
CHP2
CHP
(V0-Vccx2)
CHP3
CHP
(Vccx2)
Vcc
clk

FIG. 2 A

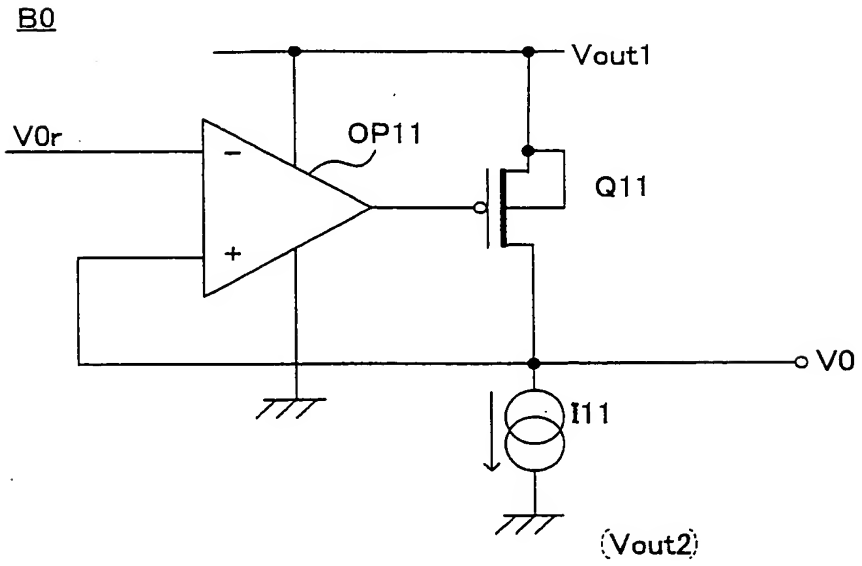

FIG. 2 B

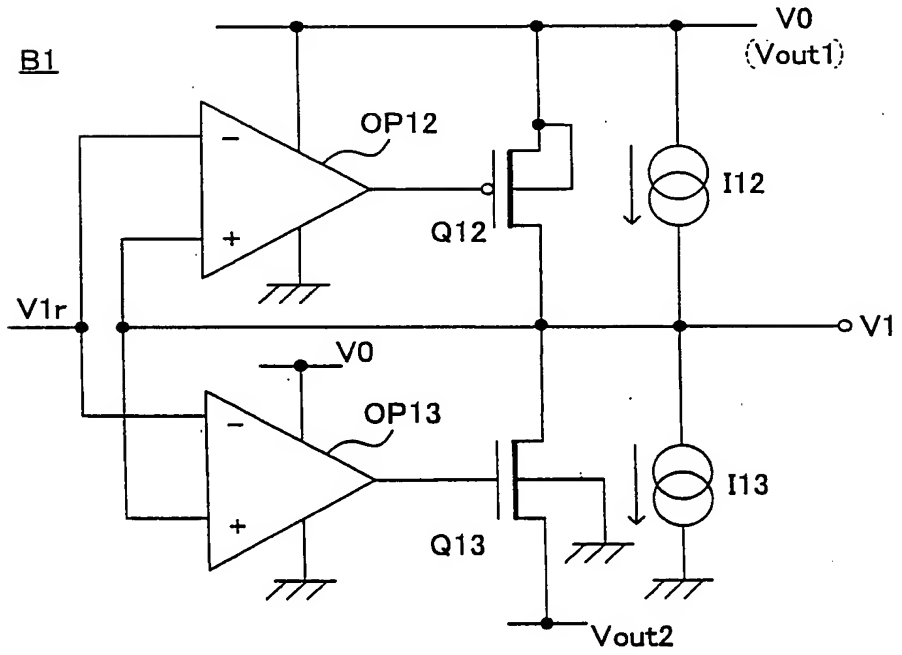

FIG. 2 C

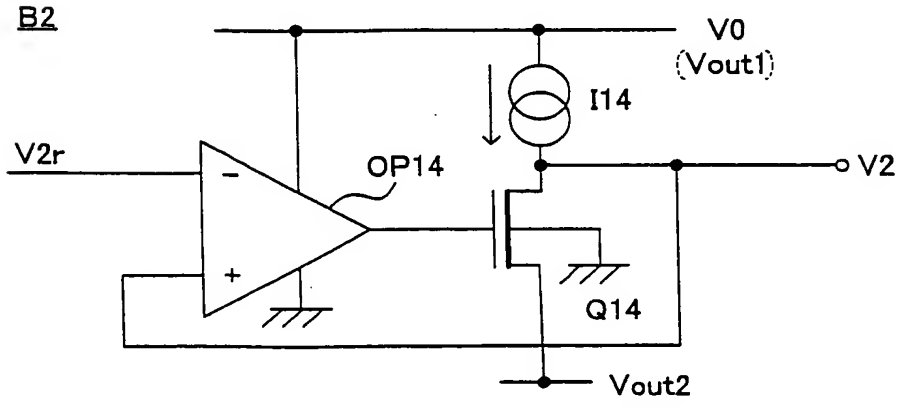

FIG. 3 A

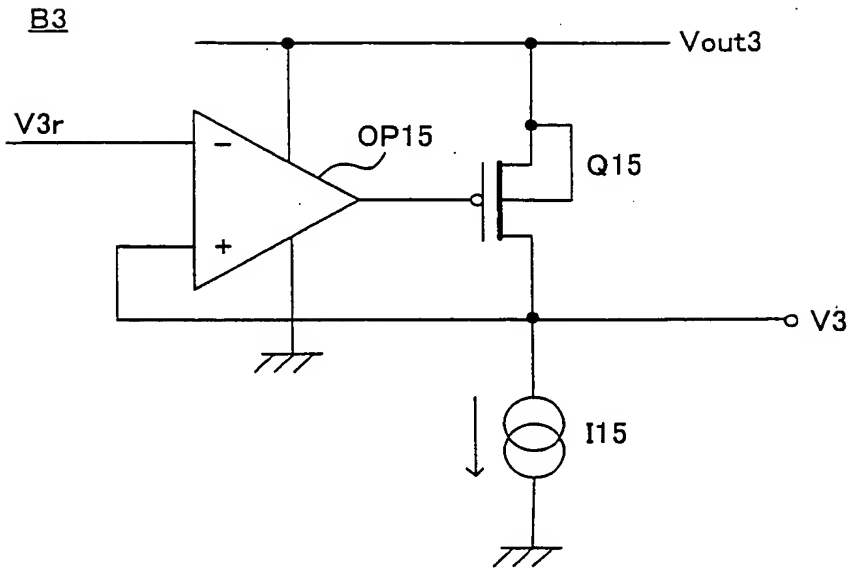
B3
Vout3
V3r
OP15
Q15
V3
I15

FIG. 3 B

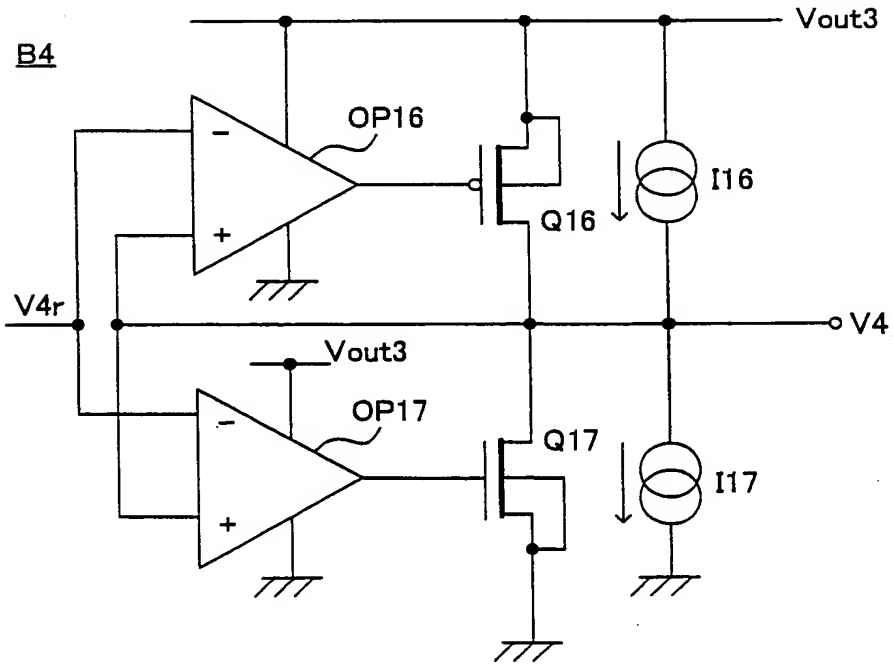
B4
Vout3
OP16
Q16
I16
V4r
V4
Vout3
OP17
Q17
I17

FIG. 4

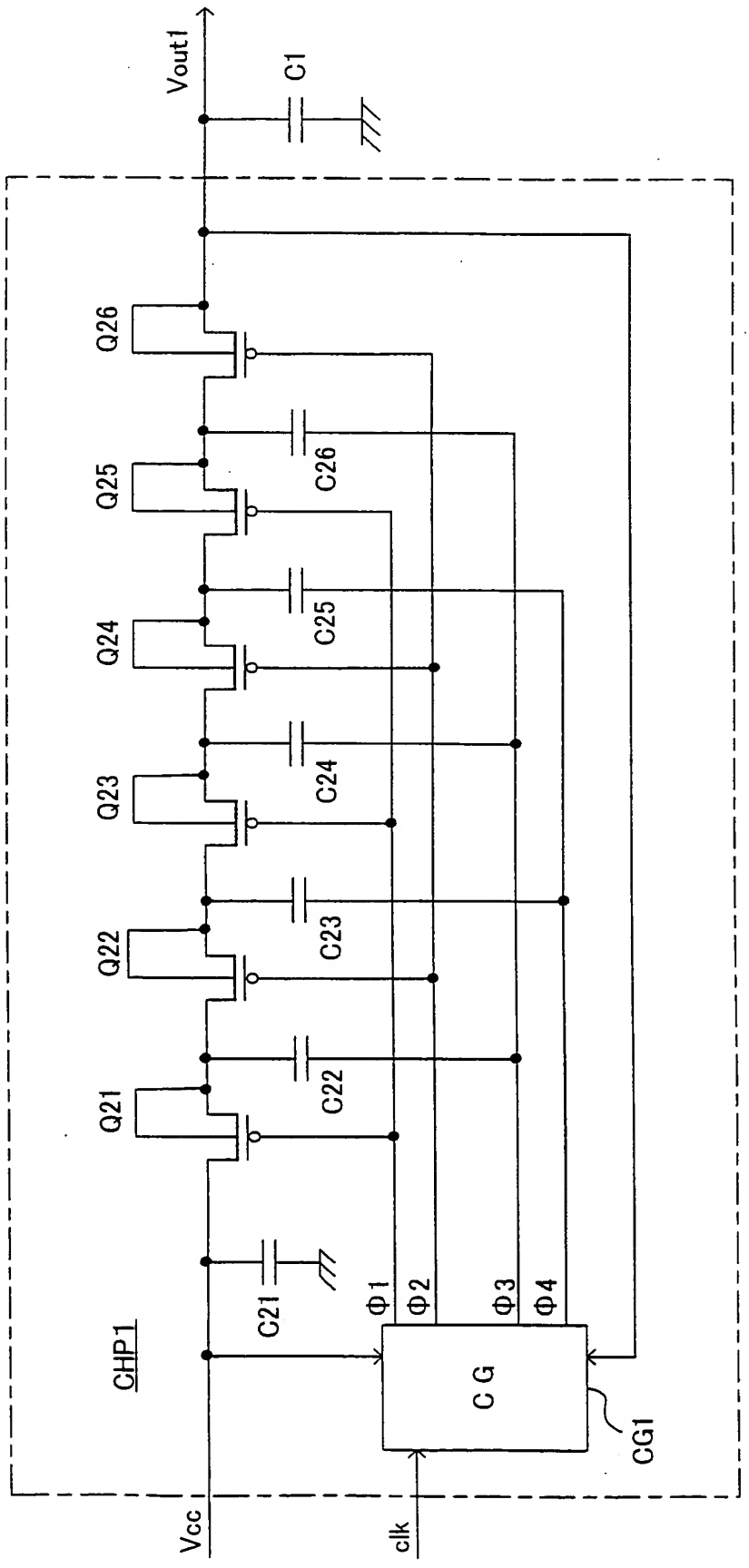
Vout1
C1
Q26
C26
Q25
C25
Q24
C24
Q23
C23
Q22
C22
Q21
C21
CHP1
Φ1
Φ2
Φ3
Φ4
C G
CG1
Vcc
clk

FIG. 5

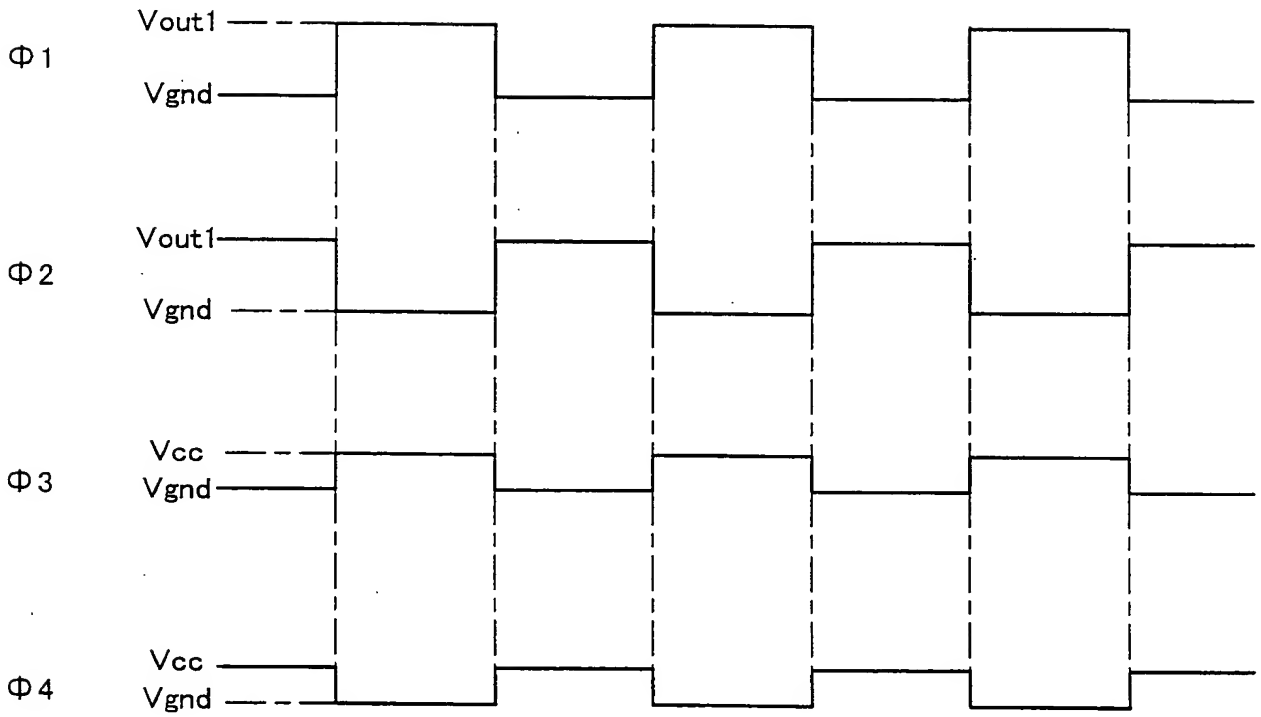

FIG. 6

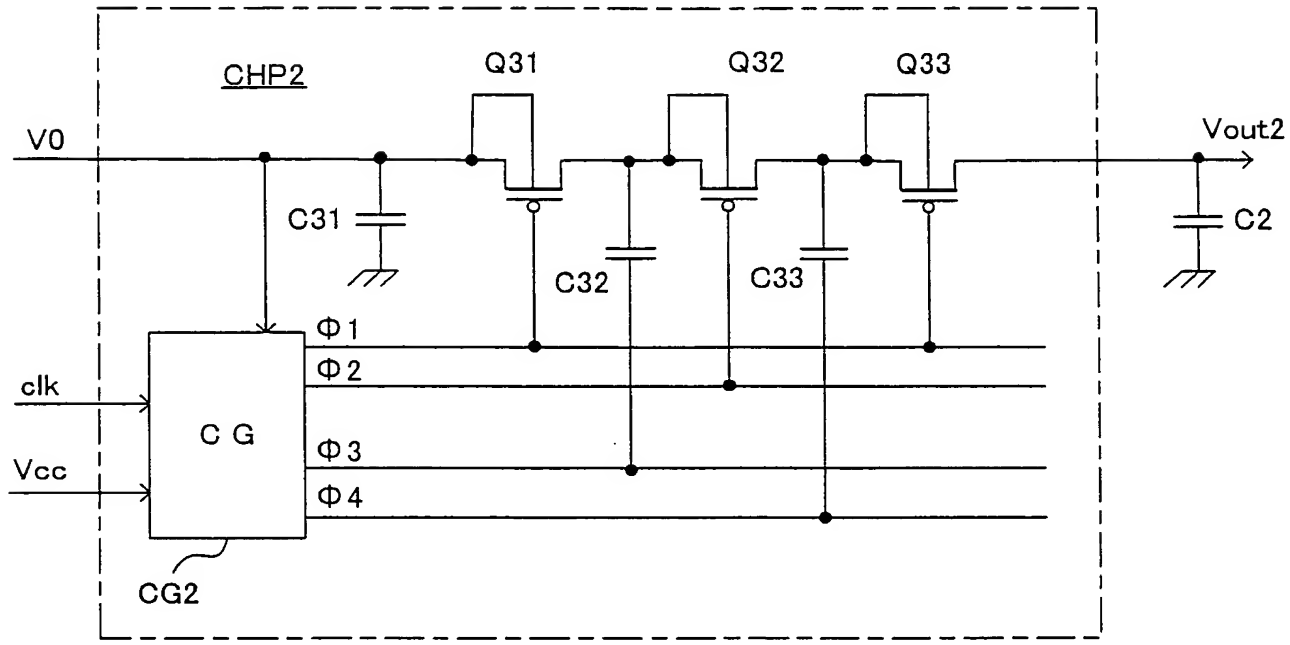
CHP2
Q31
Q32
Q33
V0
Vout2
C31
C32
C33
C2
Φ1
Φ2
Φ3
Φ4
clk
Vcc
C G
CG2

FIG. 7

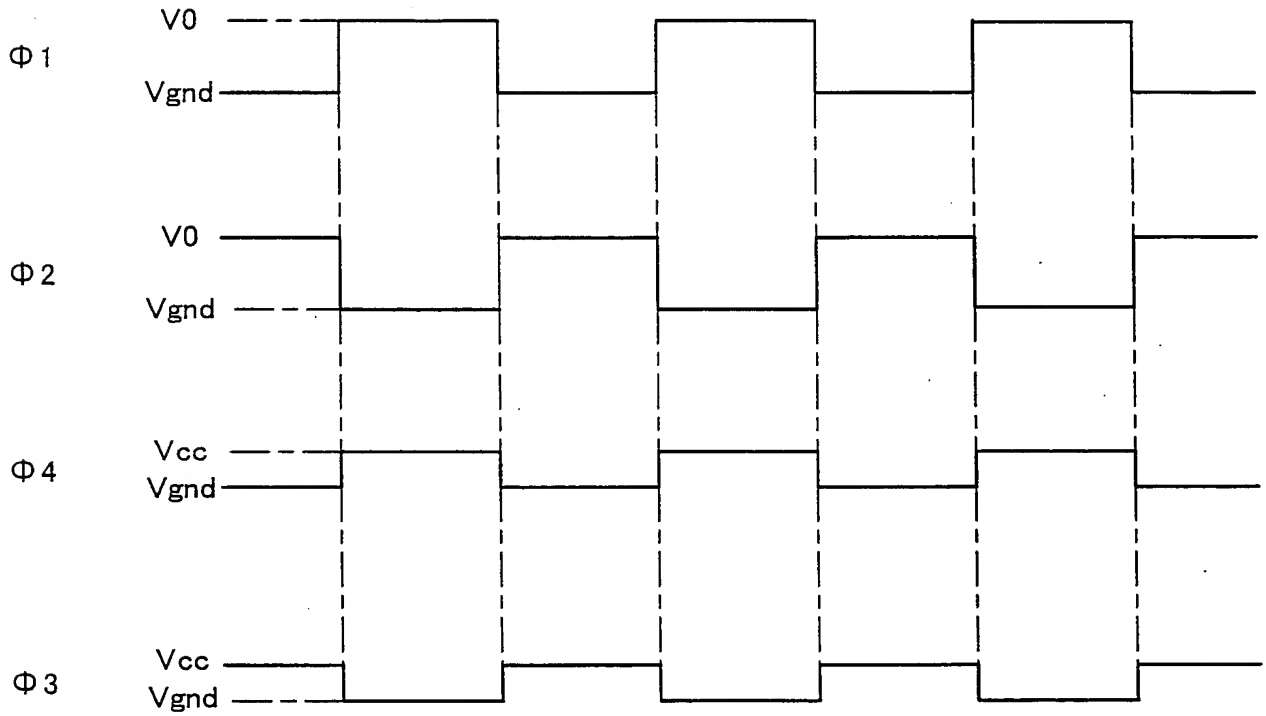

FIG. 8

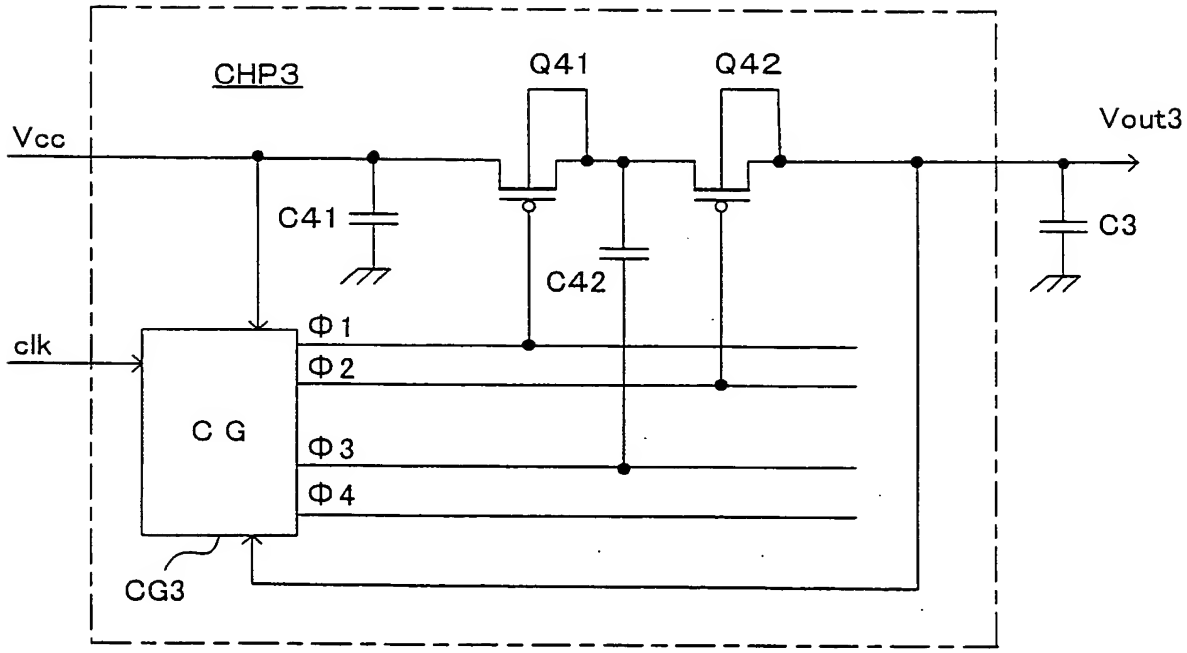

FIG. 9

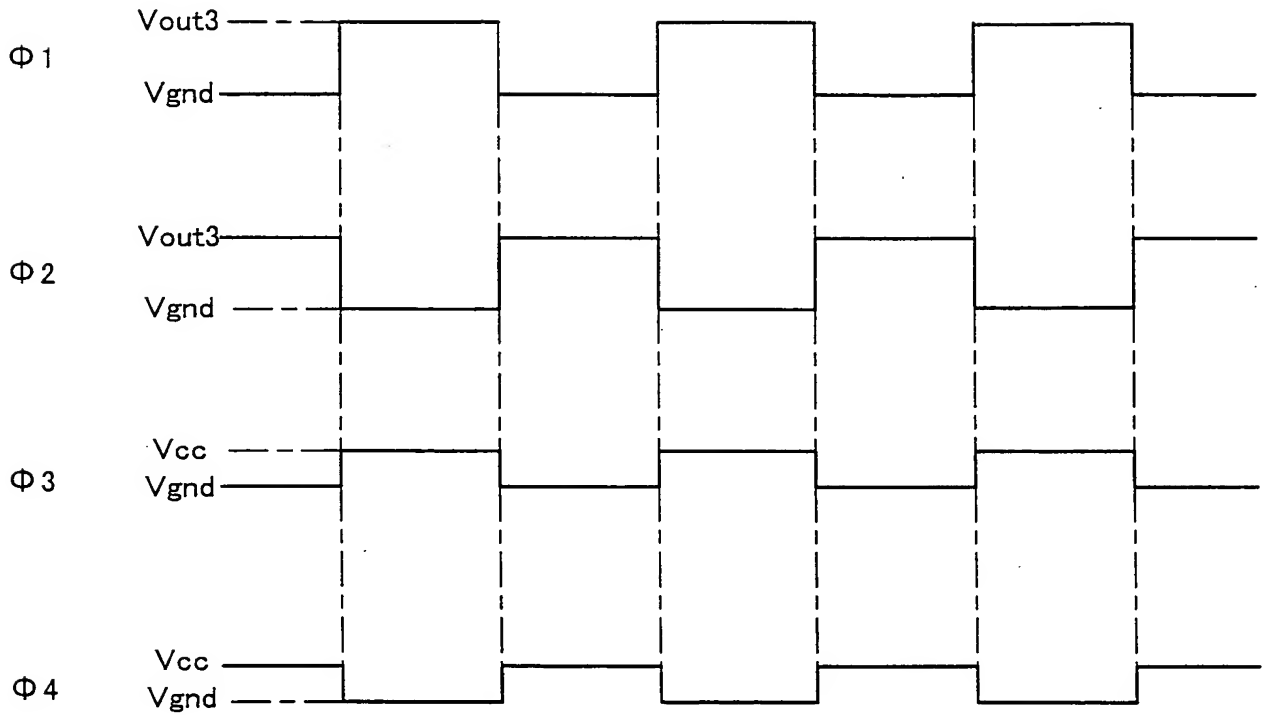

FIG. 10

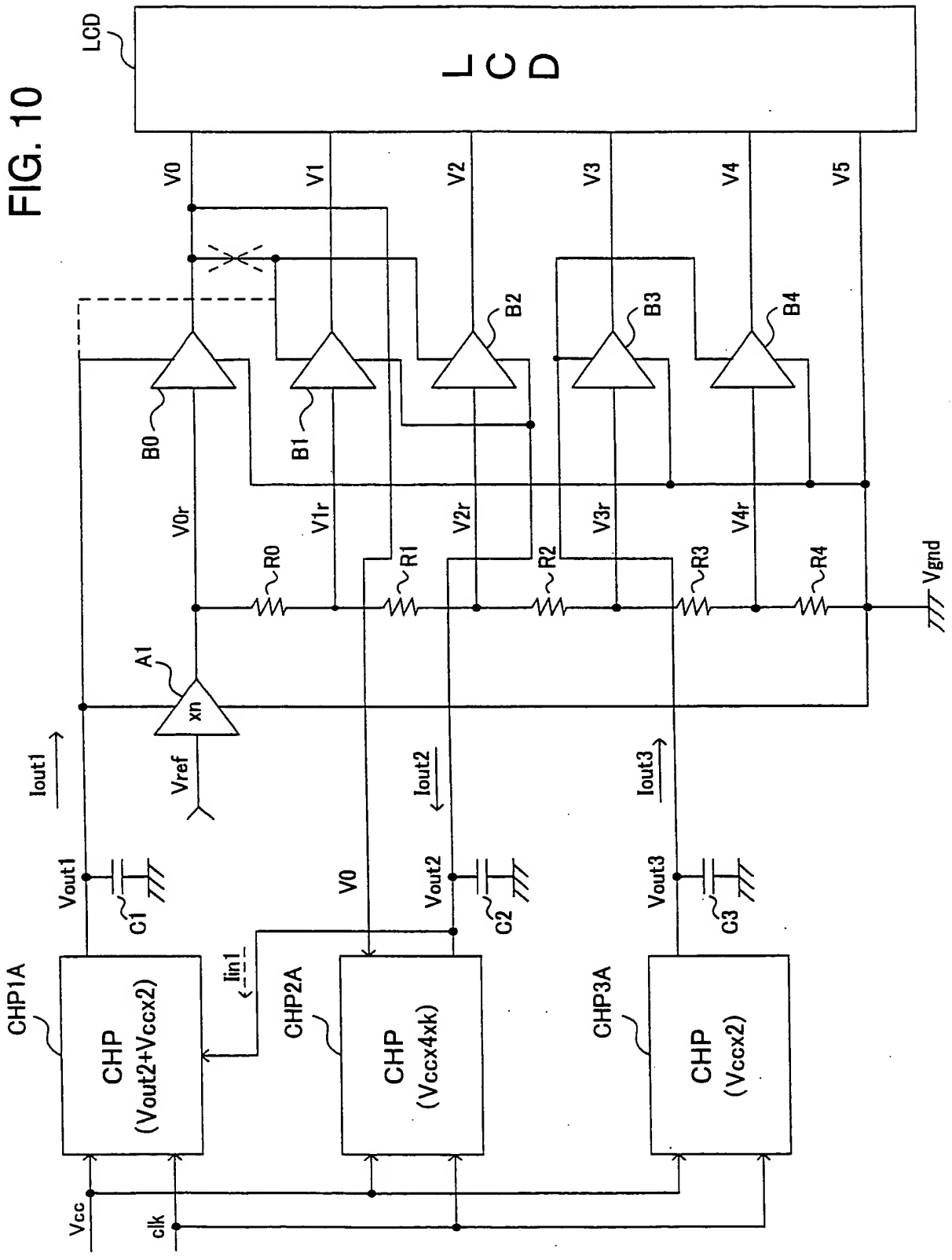
LCD
L C D
V0
V1
V2
V3
V4
V5
B0
B1
B2
B3
B4
V0r
V1r
V2r
V3r
V4r
R0
R1
R2
R3
R4
Vgnd
A1
xn
Vref
Iout1
Iout2
Iout3
Vout1
Vout2
Vout3
C1
C2
C3
V0
Iin1
CHP1A
CHP
(Vout2+Vccx2)
CHP2A
CHP
(Vccx4xk)
CHP3A
CHP
(Vccx2)
Vcc
clk

FIG. 11

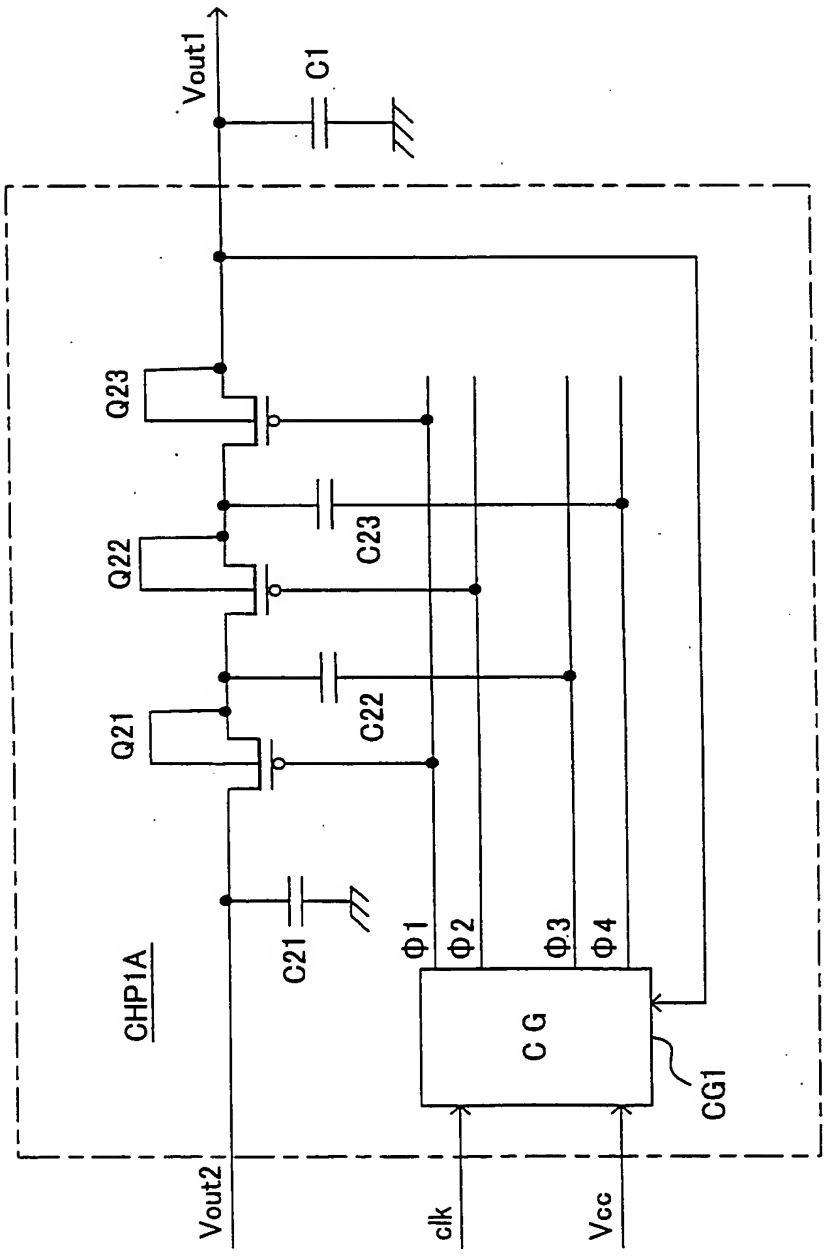
Vout1
C1
Q23
C23
Q22
C22
Q21
C21
CHP1A
Φ1
Φ2
Φ3
Φ4
C G
CG1
Vout2
clk
Vcc

FIG. 12

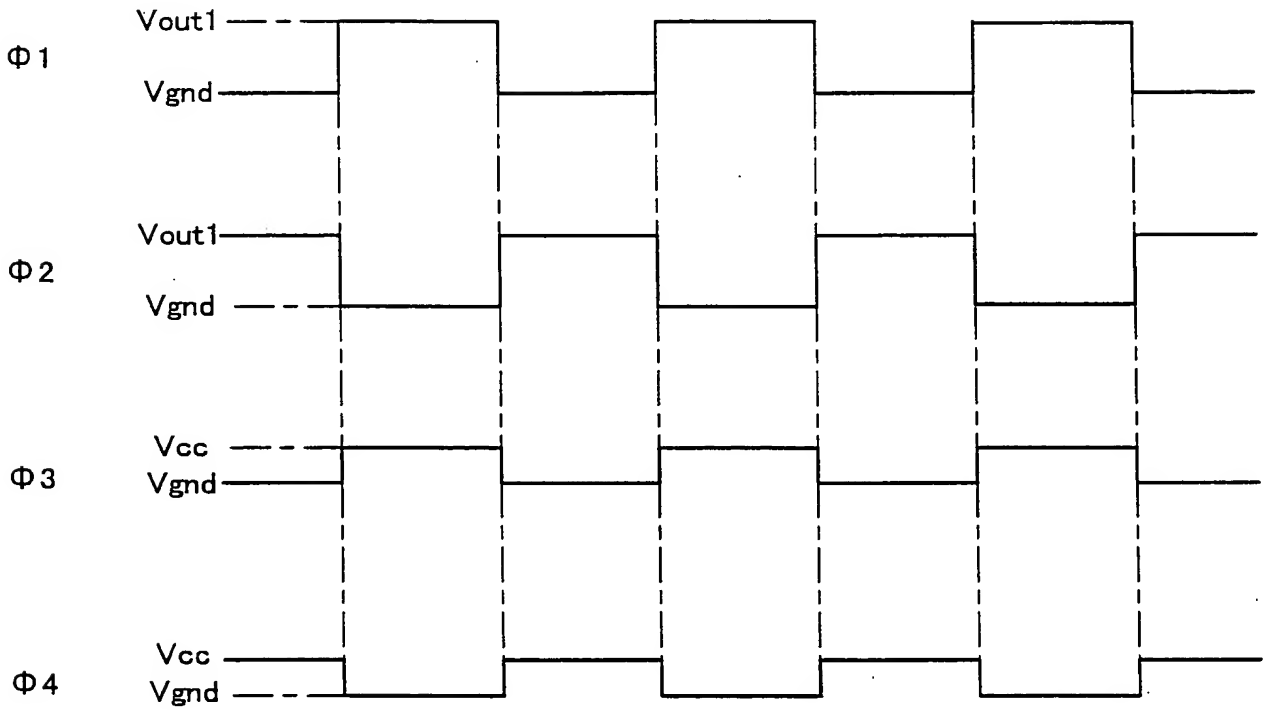

FIG. 13

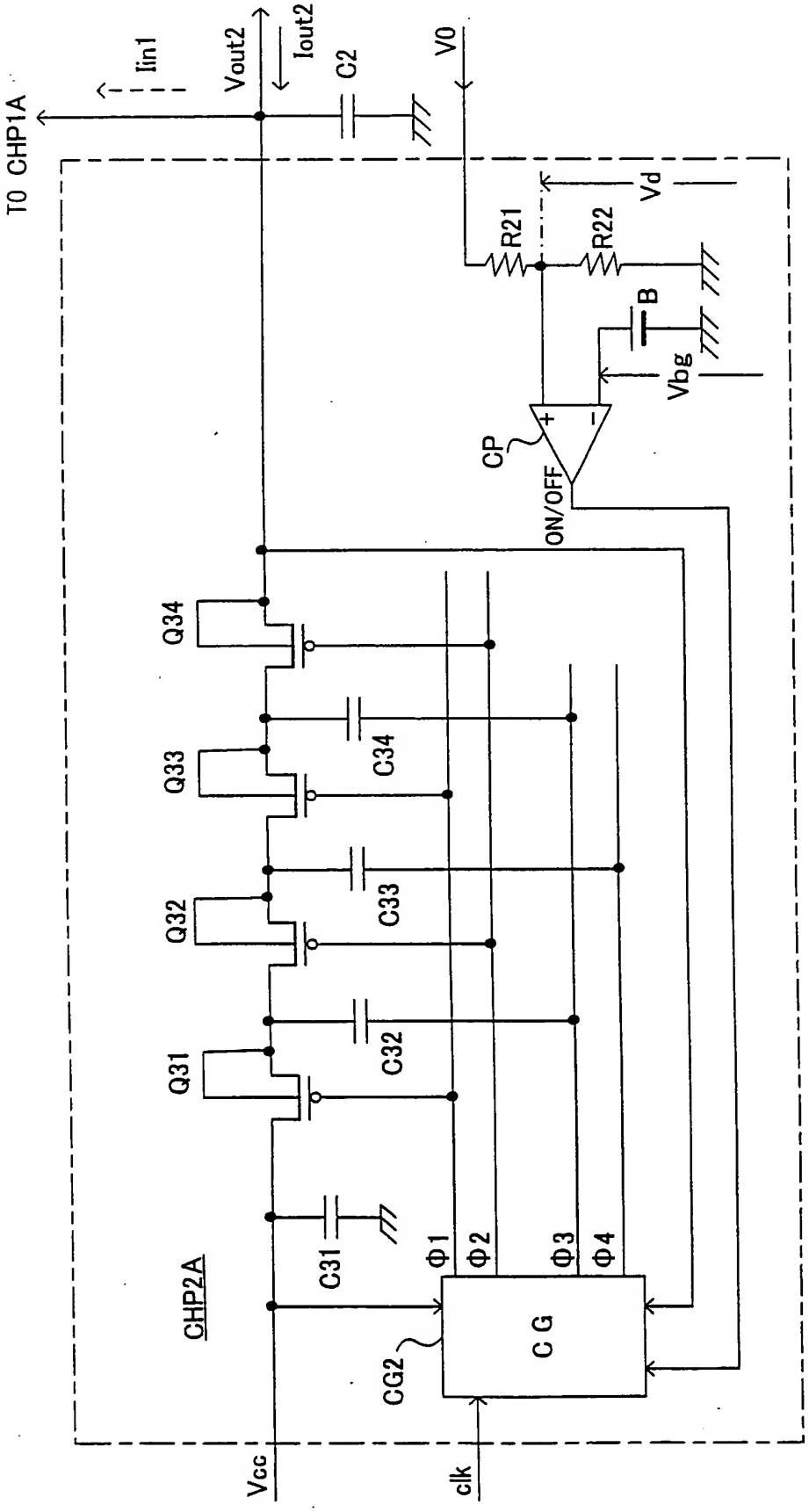
TO CHP1A
Iin1
Vout2
Iout2
C2
V0
Vd
R21
R22
B
Vbg
CP
ON/OFF
Q34
Q33
Q32
Q31
C34
C33
C32
C31
Φ1
Φ2
Φ3
Φ4
CHP2A
C G
CG2
Vcc
clk

FIG. 14

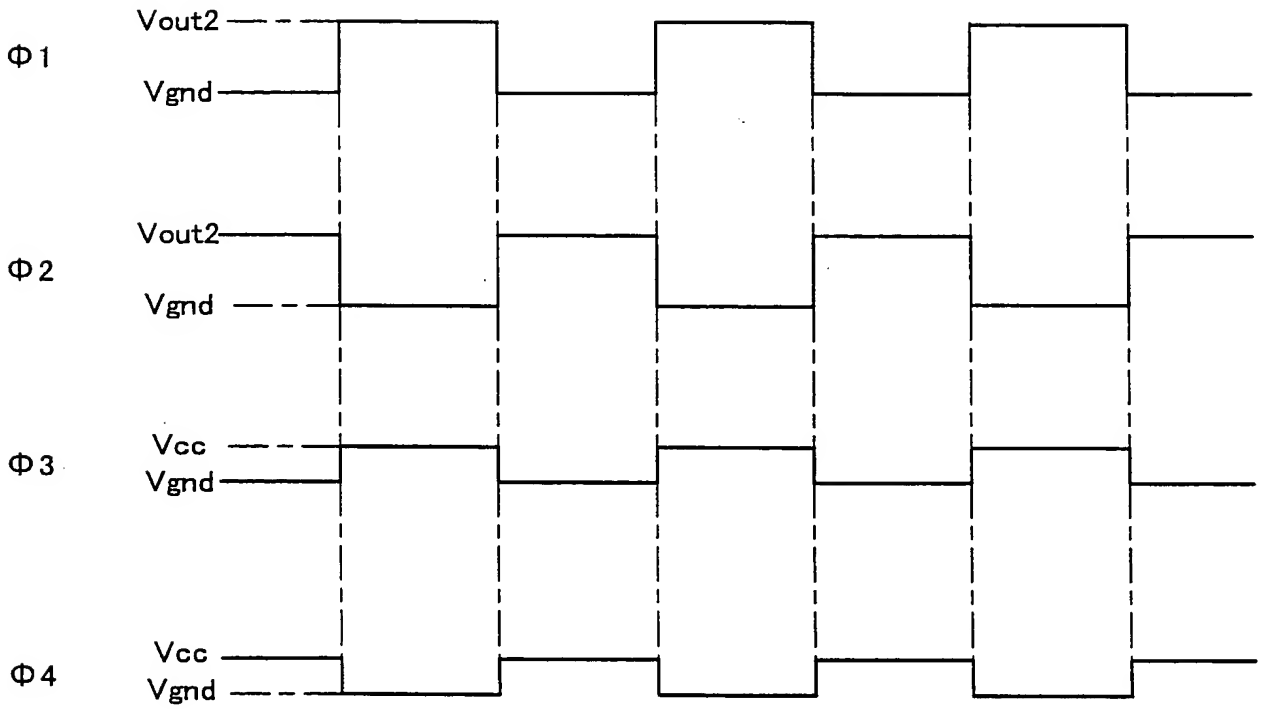

FIG. 15

PRIOR ART

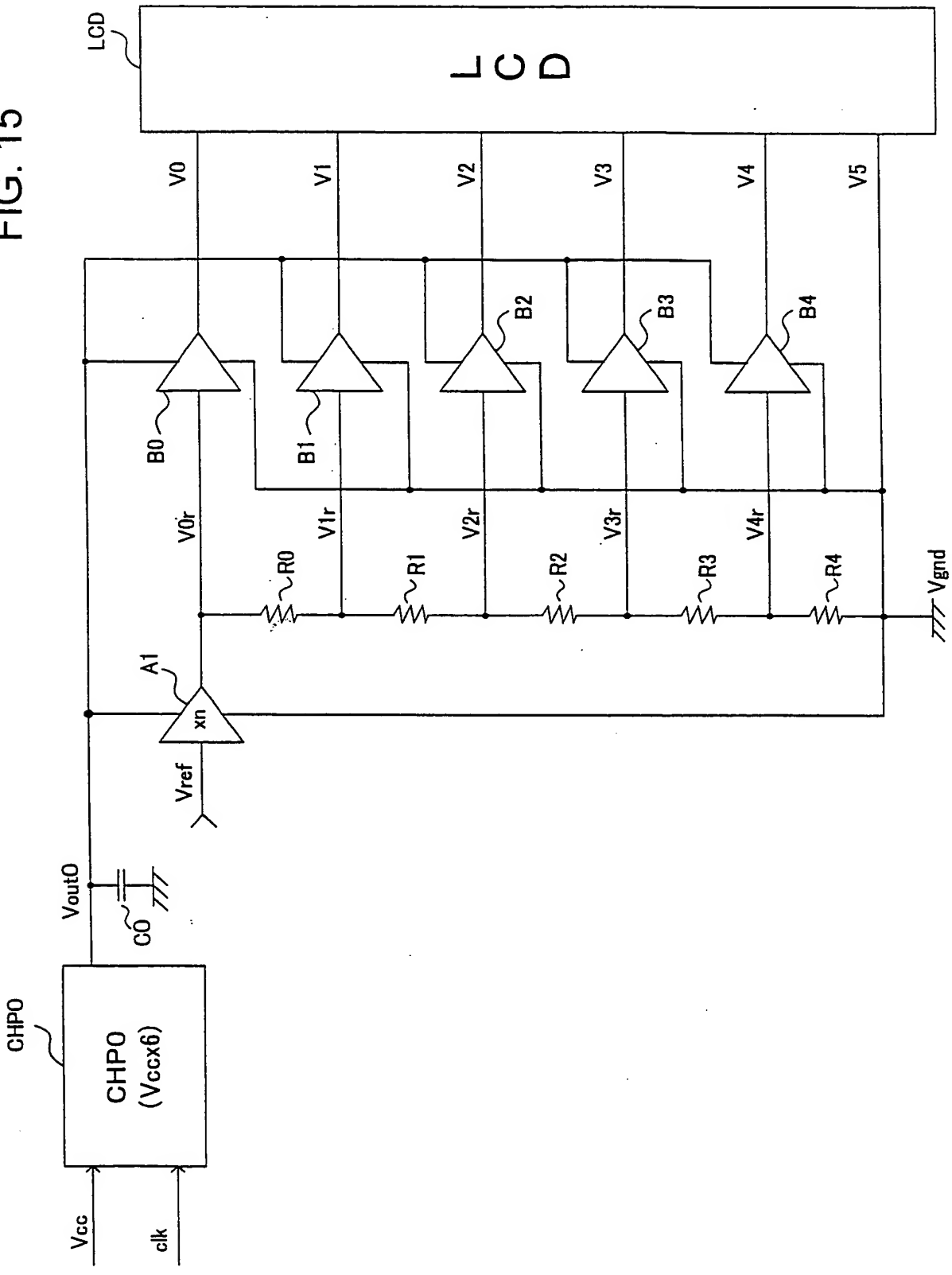

FIG. 16